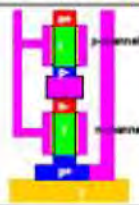
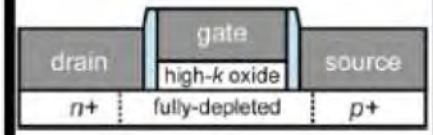
Nanoelectronics — Energy-Efficient Devices

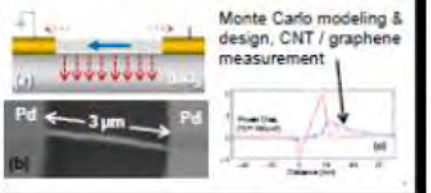
1-Dimensional nanowire interband tunnel transistors
Mayer et al. Penn State



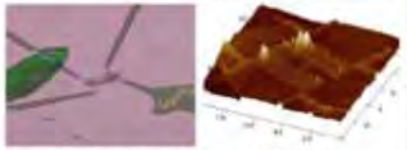
Lateral field-effect tunnel transistors
Fay et al. Notre Dame



Energy Dissipation in Non-Equilibrium 1/2-D Systems
Pop et al. Illinois

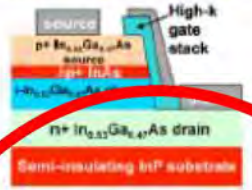


Thermal Transport and Thermal Logic Gates
Chen et al. Purdue and NML

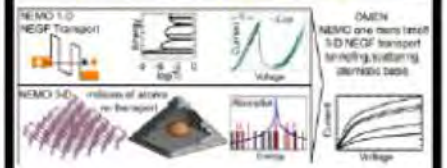


Patterned graphene nanostructures

Vertical heterostructure tunnel transistors
Datta et al. Penn State



Full 3-D, 2-D, 1-D Quantum Transport Models
Klimeck et al. Purdue

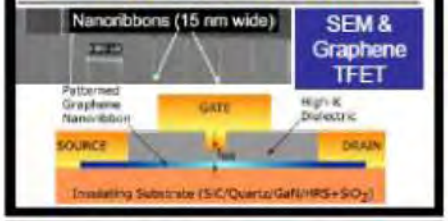


Nanoelectronics • Architectures

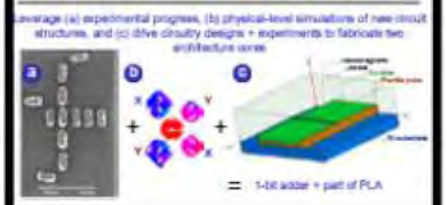
MIND

MIDWEST INSTITUTE FOR NANOELECTRONICS DISCOVERY

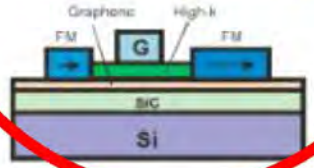
Gated graphene resonant tunneling transistors
Jena et al. Notre Dame



Architectures for nanoscale magnetic logic devices
Niemier et al. Notre Dame



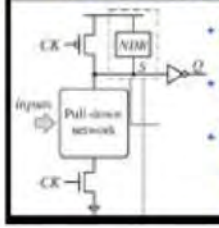
Graphene SpinFETs on Silicon
Ye et al. Purdue and UTD



Architectures for emerging NRI devices
Porod et al. Notre Dame

Provide performance comparison of NRI emerging device technologies for benchmarking and for comparison to CMOS technology

Circuit design for emerging NRI technologies
Mazumder, Univ. Michigan



- Design tunnel transistor circuits
- Enhance noise margins
- Explore multivalued and adiabatic circuits

National Lab Collaborations
NIST – Argonne – NML

Complex oxide MBE at Argonne

Architectures — Energy-Efficient Systems

INC 6